WE CLAIM:

1. An integrated circuit, comprising:

first power rails supporting a first voltage differential;

second power rails supporting a second voltage differential, wherein said second voltage differential is smaller than said first voltage differential;

a plurality of second circuits outputting a second voltage swing, wherein said second voltage swing is determined by said second voltage differential;

a plurality of signal lines, wherein said signal lines are driven by said second voltage swing; and

a plurality of regeneration circuits, wherein said regeneration circuits are receiving said second voltage swing and are outputting a first voltage swing, wherein said first voltage swing is determined by said first voltage differential.

2. The integrated circuit of claim 1, wherein in said second circuits NFET and PFET devices have low thresholds, wherein said low thresholds are lower than those thresholds which pertain to the technology of said integrated circuit.

3. The integrated circuit of claim 2, wherein in said second circuits said low thresholds are dynamically adjusted.

4. The integrated circuit of claim 1, wherein in said restoring circuits NFET and PFET devices have custom thresholds, wherein said custom thresholds are derived from said first and second voltage differentials.

5. The integrated circuit of claim 4, wherein in said restoring circuits said custom thresholds are dynamically adjusted.

6. The integrated circuit of claim 1, wherein said integrated circuit is a DRAM, and said signal lines comprise global bit-lines.

7. The integrated circuit of claim 6, wherein memory cells in said DRAM are written with said first voltage swing.

8. The integrated circuit of claim 6, further comprising interface regeneration circuits, wherein said interface regeneration circuits are receiving said second voltage swing and are outputting an interfacing voltage swing, wherein said interfacing voltage swing is larger than said second voltage swing, and wherein I/O operations in said DRAM are performed with said interfacing voltage swing.

9. The integrated circuit of claim 6, wherein said DRAM has a single ended data-line structure.

10. The integrated circuit of claim 9, wherein a Read and a subsequent WriteBack operation occurs in one cycle, wherein said integrated circuit operates in cycles.

11. The integrated circuit of claim 9, wherein a Read and a subsequent WriteBack operation occurs in more than one cycle, wherein said integrated circuit operates in cycles.

12. The integrated circuit of claim 9, further comprising a single ended primary sense amplifier with local storage and write-back capability.

13. The integrated circuit of claim 6, wherein said DRAM is an embedded DRAM macro.

14. A wide bandwidth memory, comprising:

simultaneously operable connection paths between a string of memory cells and corresponding Input/Output terminals, wherein said string of memory cells are essentially all the memory cells which are attached to the same wordline, wherein said wide bandwidth memory has a plurality of wordlines and a plurality of memory cells; and

a single ended data-line structure.

15. The wide bandwidth memory of claim 14, further comprising:

first power rails supporting a first voltage differential;

second power rails supporting a second voltage differential, wherein said second voltage differential is smaller than said first voltage differential;

a plurality of second circuits outputting a second voltage swing, wherein said second voltage swing is determined by said second voltage differential;

a plurality of signal lines, wherein said signal lines are driven by said second voltage swing; and

a plurality of regeneration circuits, wherein said regeneration circuits are receiving said second voltage swing and are outputting a first voltage swing, wherein said first voltage swing is determined by said first voltage differential.

16. The wide bandwidth memory of claim 14, wherein said wide bandwidth memory is a DRAM.

17. The wide bandwidth memory of claim 16, further comprising a single ended primary sense amplifier with local storage and write-back capability.

18. A processor, comprising:

at least one embedded memory macro, wherein said at least one embedded memory macro is further comprising:

first power rails supporting a first voltage differential;

second power rails supporting a second voltage differential, wherein said

second voltage differential is smaller than said first voltage differential;

a plurality of second circuits outputting a second voltage swing, wherein said second voltage swing is determined by said second voltage differential;

a plurality of signal lines, wherein said signal lines are driven by said second voltage swing; and

a plurality of regeneration circuits, wherein said regeneration circuits are receiving said second voltage swing and are outputting a first voltage swing, wherein said first voltage swing is determined by said first voltage differential.

19. The processor of claim 18, wherein said least one embedded memory macro has a single ended data-line structure.

20. The processor of claim 18, wherein said least one embedded memory macro is an embedded DRAM.

21. A method for conserving power in an integrated circuit, comprising the steps of:

providing said integrated circuit with power rails supporting a reduced voltage differential, wherein said reduced voltage differential is smaller than a nominal voltage differential of said integrated circuit; and

driving signal lines in said integrated circuit with a reduced voltage swing, wherein said reduced voltage swing is determined by said reduced voltage differential.

22. The method of claim 21, wherein said integrated circuit is chosen to be an embedded DRAM macro, and said signal lines are chosen to be global bit-lines.

23. The method of claim 22, wherein said embedded DRAM macro is chosen to have a single ended data-line structure.